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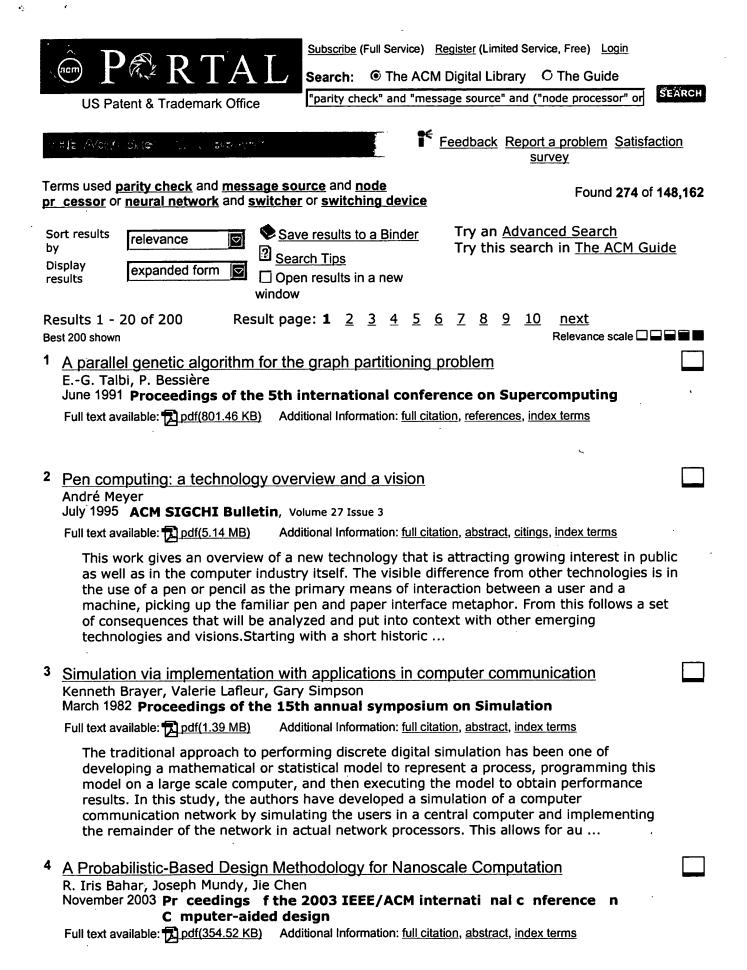
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As current silicon-based techniques fast approach their practicallimits, the investigation of nanoscale electronics, devices and system architectures becomes a central research priority. It is expected that nanoarchitectures will confront devices and interconnections with high inherent defect rates, which motivates the searchfor new architectural paradigms. In this paper, we propose a probabilistic-based design methodology for designing nanoscale computer architectures based on Markov Random Fields (M ...

	compact dicinestrates based on larkey Random Floras (11 m	
5	98¢/Mflops/s ultra-large-scale neural-network training on a plll cluster Douglas A. Aberdeen, Jonathan Baxter, Robert Edwards November 2000 Proceedings of the 2000 ACM/IEEE conference on Supercomputing (CDROM) Full text available: pdf(215.33 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms	
	Artificial neural networks with millions of adjustable parameters and a similar number of training examples are a potential solution for difficult, large-scale pattern recognition problems in areas such as speech and face recognition, classification of large volumes of web data and finance. The bottleneck is that neural network training involves iterative gradient descent and is extremely computationally intensive. In this paper we present a technique for distributed training of Ultra Large	
	Keywords: neural-network, Linux cluster, matrix-multiply	
6	Neural networks and dynamic complex systems	
	Geoffrey Fox, Wojtek Furmanski, Alex Ho, Jeff Koller, Peter Simic, Isaac Wong March 1989 Proceedings of the 22nd annual symposium on Simulation	
	Full text available: pdf(1.44 MB) Additional Information: full citation, abstract, references, index terms	
	We describe the use of neural networks for optimization and inference associated with a variety of complex systems. We show how a string formalism can be used for parallel computer decomposition, message routing and sequential optimizing compilers. We extend these ideas to a general treatment of spatial assessment and distributed artificial intelligence.	
7	An architecture for extended abstract data flow	Г
	Vason P. Srini May 1981 Proceedings of the 8th annual symposium on Computer Architecture	
	Full text available: pdf(1.12 MB) Additional Information: full citation, abstract, references, citings, index terms	
	A distributed computer system environment for executing extended abstract data flow graphs (EDFGs) is presented. Sequencing functions in EDFGs depends on the availability of data. Since the functions are free of side effects, unrelated functions can be executed in parallel if the required data is available. The environment comprises an organization of conventional or data flow processors and the kernel functions of a distributed operating system. The processors are organized in g	
8	Architectures: A perspective on the future of massively parallel computing: fine-grain	
	vs. coarse-grain parallel models comparison & contrast	
	Predrag T. Tosic April 2004 Pr ceedings f the first c nference n c mputing fr ntiers n C mputing fr ntiers	
	Full text available: pdf(277.49 KB) Additional Information: full citation, abstract, references, index terms	
	Models, architectures and languages for parallel computation have been of utmost research	

interest in computer science and engineering for several decades. A great variety of parallel computation models has been proposed and studied, and different parallel and distributed architectures designed as some possible ways of harnessing parallelism and improving performance of the general purpose computers. Massively parallel connectionist models such as artificial neural networks (...

Keywords: cellular automata, distributed systems, massively parallel computing, multiprocessor computers, neural networks, parallel computation models

9	What have we learnt from using real parallel machines to solve real problems? G. C. Fox	
	January 1989 Proceedings of the third conference on Hypercube concurrent computers and applications - Volume 2	
	Full text available: pdf(4.08 MB) Additional Information: full citation, abstract, references, citings, index terms	
	We briefly review some key scientific and parallel processing issues in a selection of some 84 existing applications of parallel machines. We include the MIMD hypercube transputer array, BBN Butterfly, and the SIMD ICL DAP, Goodyear MPP and Connection Machine from Thinking Machines. We use a space-time analogy to classify problems and show how a division into synchronous, loosely synchronous and asynchronous problems is helpful. This classifies problems into those suitable for SIMD or MIMD	
10	Load balancing loosely synchronous problems with a neural network	
	G. C. Fox, W. Furmanski January 1988 Proceedings of the third conference on Hypercube concurrent computers and applications: Architecture, software, computer systems, and general issues - Volume 1	
	Full text available: pdf(2.90 MB) Additional Information: full citation, abstract, references, citings, index terms	
	Hopfield and Tank have introduced the use of neural networks for the solution of optimization problems such as the traveling salesman problem. Here we show how to generalize this method to decompose loosely synchronous problems onto parallel machines and in particular the hypercube. In this case, decomposition or load balancing can be formulated graph theoretically in terms of optimal partitioning of the computational graph into $N=2$	
11	Identification of parallelism in neural networks by simulation with language J.	
	Alexei N. Skurihin, Alvin J. Surkan September 1993 ACM SIGAPL APL Quote Quad, Proceedings of the international conference on APL, Volume 24 Issue 1	
	Full text available: pdf(588.94 KB) Additional Information: full citation, abstract, references, citings, index terms	
	Neural networks, trained by backpropagation, are designed and described in the language J , an APL derivative with powerful function encapsulation features. Both the languages J [4,6,7] and APL [5] help to identify and isolate the parallelism that is inherent in network training algorithms. Non-critical details of data input and derived output processes are deemphasized by relegating those functions to callable stand-alone modules. Such input and output	
12	A constructive algorithm for neural networks that generalize Alvin Surkan, Colin Campbell January 1998 ACM SIGAPL APL Qu te Quad, Pr ceedings f the c nference n Share kn wledge share success, Volume 28 Issue 4 Full text available: pdf(650.04 KB) Additional Information: full citation, abstract, index terms	
	run text available. Tag pultopulus ND) — Additional miormation: <u>idii citation, abstract, ind</u> ex terms	

APL functions were designed to describe a constructive algorithm that synthesizes a neural network while optimizing its ability to generalize. Algorithms are implemented in programs to discover networks of binary weights that assign unfamiliar, high-dimension binary patterns to their most similar classes. Constructive algorithms that create networks are important for the design of classifiers based on array-processors made from fast two-level circuits. APL is an effective tool for the exposition ...

	circuits. Art is all effective tool for the exposition	
13	Ariel: a scalable multiprocessor for the simulation of neural networks Gary Frazier	
	March 1990 ACM SIGARCH Computer Architecture News, Volume 18 Issue 1	
	Full text available: pdf(729.87 KB) Additional Information: full citation, abstract, index terms	
	Ariel is a multiprocessor architecture that we are developing to simulate neural networks and other models of distributed computation. The design is based upon a hierarchical network of coarse-grained processing modules. The module hardware uses fast digital signal processors and very large semiconductor memories to provide the throughput and storage capacity required to simulate large networks. Our objective is to provide a system that can be scaled up to simulate neural networks compose	
14	Critical issues in mapping neural networks on message-passing multicomputers J. Ghosh, K. Hwang	
	May 1988 ACM SIGARCH Computer Architecture News, Proceedings of the 15th	
	Annual International Symposium on Computer architecture, Volume 16 Issue 2 Full text available: pdf(1.05 MB) Additional Information: full citation, abstract, references, index terms	
	Connectionist models such as artificial neural systems, offer an intrinsically concurrent computational paradigm. We investigate the architectural requirements for efficiently simulating large neural networks on a multicomputer system with thousands of fine-grained processors and distributed memory. First, models for characterizing the structure of a neural network and the function of individual cells are developed. These models provide guidelines for efficiently mapping the network onto mu	
15	High speed neural network chip for trigger purposes in high energy physics W. Eppler, T. Fischer, H. Gemmeke, A. Menchikov	
	February 1998 Proceedings of the conference on Design, automation and test in Europe	
	Full text available: pdf(116.42 KB) Additional Information: full citation, abstract, references, index terms Additional Information: full citation, abstract, references, index terms	
	A novel neural chip SAND (Simple Applicable Neural Device) is described. It is highly usable for hardware triggers in particle physics. The chip is optimized for a high input data rate (50 MHz, 16 bit data) at a very low cost basis. The performance of a single SAND chip is 200 MOPS due to four parallel 16 bit multipliers and 40 bit adders working in one clock cycle. The chip is able to implement feedforward neural networks with a maximum of 512 input neurons and three hidden layers. Kohonen feat	
	Keywords : VME board with neural network chip SAND, Hardware accelerator for neural networks, High energy physics: trigger, on- and off-line analysis	
16	Transparent remote execution in LAHNOS by means of a neural network device M. Cena, M. L. Crespo, R. Gallard January 1995 ACM SIGOPS Operating Systems Review, Volume 29 Issue 1	
	Full text available: pdf(596.41 KB) Additional Information: full citation, abstract, index terms	
	LAHNOS is a Local Area Heterogeneous Operating System [1] being currently developed at	
	the Universidad Nacional de San Luis over which distributed services are to be built. This	

paper shows some enhancements to be introduced into the original design in order to achieve automatic allocation of remote execution requests to the best fitted node under some chosen performance criteria. Following current trends in Distributed Systems we propose the insertion of a neural network device into the kernel o ...

Keyw rds: neural networks, operating system, workload

17 Mark IIIfp hypercube concurrent processor architecture	
J. Tuazon, J. Peterson, M. Pniel	
January 1988 Proceedings of the third conference on Hypercube concurrent computers	
and applications: Architecture, software, computer systems, and general issues - Volume 1	
Full text available: pdf(1.02 MB) Additional Information: full citation, abstract, references, citings, index terms	
The Mark Illfp Hypercube is a new generation of hypercube concurrent processor system developed at JPL/Caltech, with peak performance of 5 Mips, 14 Mflops per node, and a peak communication rate of 6 Mbytes per second. Each node utilizes two Motorola MC68020 microprocessors, an MC68882 scalar floating- point coprocessor, and a Weitek 8000 floating-point chip set. One of the MC68020 processors serves as the application and computational processor, the other is dedicated to communication. The	
18 A survey of commercial parallel processors Edward Gehringer, Janne Abullarade, Michael H. Gulyn September 1988 ACM SIGARCH Computer Architecture News, Volume 16 Issue 4	
Full text available: pdf(2.96 MB) Additional Information: full citation, abstract, citings, index terms	
This paper compares eight commercial parallel processors along several dimensions. The processors include four shared-bus multiprocessors (the Encore Multimax, the Sequent Balance system, the Alliant FX series, and the ELXSI System 6400) and four network multiprocessors (the BBN Butterfly, the NCUBE, the Intel iPSC/2, and the FPS T Series). The paper contrasts the computers from the standpoint of interconnection structures, memory configurations, and interprocessor communication. Also, the share	
19 X-Tree: A tree structured multi-processor computer architecture Alvin M. Despain, David A. Patterson April 1978 Proceedings of the 5th annual symposium on Computer architecture	
Full text available: pdf(535.88 KB) Additional Information: full citation, abstract, references, citings, index terms	
The problem of organizing multiple, monolithic microprocessors into an effective general purpose computer structure is examined. A tree structure with extra interconnections was found to be especially attractive. It provides a structured hierarchy for control, addressing and message routing. More important, it appears to provide a mechanism to automatically migrate data abstractions and processes over the network of processors. The network can be expanded to any desired size and no global c	
Multiprocessor simulation of neural networks with NERV R. Manner, R. Horner, R. Hauser, A. Genthner August 1989 Pr ceedings f the 1989 ACM/IEEE c nference n Superc mputing	
Full text available: pdf(1.08 MB) Additional Information: full citation, abstract, references, index terms	
A general-purpose simulation system for neural networks is computationally very demanding. This paper presents some estimations of the computing power required, the necessary interconnection bandwidth, and the requisite memory size. Next, the hardware	

architecture of the NERV multiprocessor system is derived that fulfills these requirements.

Up to 320 processors 68020 are used in a single VME crate together with a Macintosh II as a host computer. This set-up provides a computing power of 13 ...

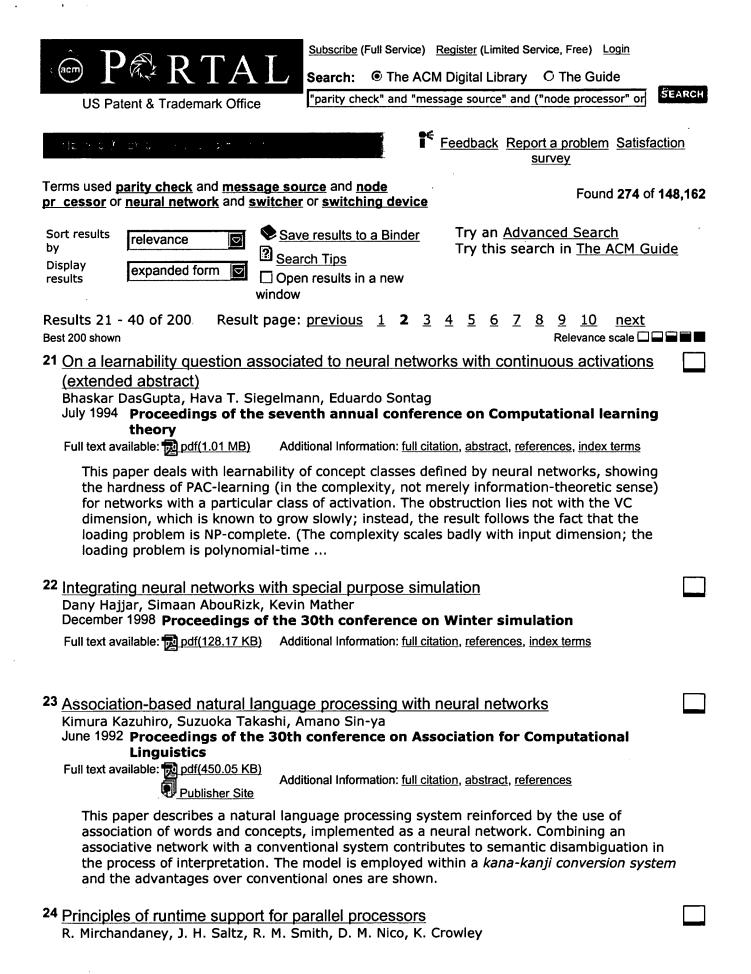
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June 1988 Pr ceedings f the 2nd internati nal c nference n Superc mputing Additional Information: full citation, abstract, references, citings, index Full text available: Dodf(1.32 MB) terms

There exists substantial data level parallelism in scientific problems. The PARTY runtime system is an attempt to obtain efficient parallel implementations for scientific computations, particularly those where the data dependencies are manifest only at runtime. This can preclude compiler based detection of certain types of parallelism. The automated system is structured as follows: An appropriate level of granularity is first selected for the computations. A directed acyclic graph represent ...

25 Session 9A: System level test and reliability: Accurate CMOS bridge fault modeling	
with neural network-based VHDL saboteurs	
Don Shaw, Dhamin Al-Khalili, Côme Rozon	
November 2001 Proceedings of the 2001 IEEE/ACM international conference on	
Computer-aided design	
Full text available: pdf(137.79 KB) Additional Information: full citation, abstract, references, citings, index	

This paper presents a new bridge fault model that is based on a multiple layer feedforward neural network and implemented within the framework of a VHDL saboteur cell. Empirical evidence and experimental results show that it satisfies a prescribed set of bridge fault model criteria better than existing approaches. The new model computes exact bridged node voltages and propagation delay times with due attention to surrounding circuit elements. This is significant since, with the exception of full ...

<u>terms</u>

Keywords: CMOS ICs, VHDL, bridge defects, fault models, fault simulation, neural networks

26 Problems and approaches for a Teraflop processor

A. H. Frey, G. C. Fox

January 1988 Proceedings of the third conference on Hypercube concurrent computers and applications: Architecture, software, computer systems, and general issues - Volume 1

Full text available: pdf(463.59 KB) Additional Information: full citation, abstract, references, index terms

This paper discusses problems associated with designing a processor capable of sustaining a teraflop (1012 floating point operations per second) of processing power. Several researcher have speculated on achieving this performance. The technical problems of a practical design are shown to be formidable. However, none of these problems requires a technology breakthrough for their solution. The predictable advances of the next generation of technology together with a majo ...

27 Embedded systems: Accurate software performance estimation using domain classification and neural networks

Márcio Seiji Oyamada, Felipe Zschornack, Flávio Rech Wagner

September 2004 Proceedings of the 17th symposium on Integrated circuits and system design

Full text available: pdf(137.87 KB) Additional Information: full citation, abstract, references, index terms

For the design of an embedded system, there is a variety of available processors, each one offering a different trade-off concerning factors such as performance and power consumption. High-level performance estimation of the embedded software implemented in a particular architecture is essential for a fast design space exploration, including the choice of the most appropriate processor. However, advanced architectures present many features, such as deep pipelines, branch prediction mechanisms an ...

Keyw rds: embedded software, neural networks, performance estimation 28 Optimal communication algorithms for regular decompositions on the hypercube G. C. Fox, W. Furmanski January 1988 Proceedings of the third conference on Hypercube concurrent computers and applications: Architecture, software, computer systems, and general issues - Volume 1 Additional Information: full citation, abstract, references, citings, index Full text available: pdf(4.81 MB) terms We discuss optimal communication and decomposition algorithms for a class of regular problems on concurrent computers with a hypercube topology, using a general technique we call the method of cube geodesics. We address the calculation of various transformations (convolutions, functionals etc.) of data distributed over the hypercube; examples are the Fast Fourier Transform, matrix algorithms, global scalar products and vector sums, sorting. These all involve long distance inter ... 29 Fuzzy RuleNet: an artificial neural network model for fuzzy classification Nadine Tschichold-Gürman April 1994 Proceedings of the 1994 ACM symposium on Applied computing Full text available: pdf(571.46 KB) Additional Information: full citation, references, index terms 30 A QoS-Provisioning neural fuzzy connection admission controller for multimedia highspeed networks Ray-Guang Cheng, Chung-Ju Chang, Li-Fong Lin February 1999 IEEE/ACM Transactions on Networking (TON), Volume 7 Issue 1 Full text available: pdf(342.90 KB) Additional Information: full citation, references, citings, index terms 31 Interprocessor communication speed and performance in distributed-memory parallel processors M. Annaratone, C. Pommerell, R. Rühl April 1989 ACM SIGARCH Computer Architecture News, Proceedings of the 16th annual international symposium on Computer architecture, Volume 17 Issue 3 Additional Information: full citation, abstract, references, citings, index Full text available: pdf(1.27 MB) terms We have simulated several numerical and non-numerical algorithms on five distributedmemory parallel processors (DMPPs). All five DMPPs have the same topology (a torus), and the same number of nodes. The architectures differ only in the communication speed between neighboring nodes, while the computation unit is kept unchanged. The goal of the paper is to quantify the effect that interprocessor communication speed and synchronization overhead have on the performance of the DMPPs. Af ... 32 Software protection: Attacks and risk analysis for hardware supported software copy protection systems Weidong Shi, Hsien-Hsin S. Lee, Chenghuai Lu, Tao Zhang October 2004 Pr ceedings f the 4th ACM w rksh p n Digital rights management Full text available: pdf(167.21 KB) Additional Information: full citation, abstract, references, index terms <i>Recently, there is a growing interest in the research community to use tamper-resistant

processors for software copy protection. Many of these tamper-resistant systems rely on a specially tailored secure processor to prevent, 1) illegal software duplication, 2) unauthorized software modification, and 3)unauthorized software reverse engineering. The published techniques primarily focused on feasibility demonstration and design details rather than analyzing security risks and potential a ...

Keywords: attack, copy protection, tamper resistance

33 Hypermedia & TAL: Semantic Network Array Processor as a massively parallel computing platform for high performance and large-scale natural language processing	
Hiroaki Kitano, Dan Moldovan August 1992 Proceedings of the 14th conference on Computational linguistics - Volume 2	:
Full text available: pdf(582.00 KB) Additional Information: full citation, abstract, references	
This paper demonstrates the utility of the Semantic Network Array Processor (SNAP) as a massively parallel platform for high performance and large-scale natural language processing systems. SNAP is an experimental massively parallel machine which is dedicated to, but not limited to, the natural language processing using semantic networks. In designing the SNAP, we have investigated various natural language processing systems and theories to determine the scope of the hardware support and a set o	
34 Experiences with non-numeric applications on multithreaded architectures Angela Sodan, Guang R. Gao, Olivier Maquelin, Jens-Uwe Schultz, Xin-Min Tian	
June 1997 ACM SIGPLAN Notices, Proceedings of the sixth ACM SIGPLAN symposium	
on Principles and practice of parallel programming, Volume 32 Issue 7	
Full text available: pdf(1.32 MB) Additional Information: full citation, abstract, references, citings, index terms	
Distributed-memory machines have proved successful for many challenging numerical programs that can be split into largely independent computation-intensive subtasks requiring little data exchange (although the amount of exchanged data may be large). However, many irregular applicationse.g. in the AI field have a fairly tight data coupling that often results from the use of shared data structures, making them in many cases not amenable to parallelization on distributed-memory machines. EAR	
35 On the computational power of neural nets	
Hava T. Siegelmann, Eduardo D. Sontag July 1992 Proceedings of the fifth annual workshop on Computational learning theory	, <u> </u>
Full text available: pdf(1.02 MB) Additional Information: full citation, abstract, references, citings, index terms	
This paper deals with finite networks which consist of interconnections of synchronously evolving processors. Each processor updates its state by applying a "sigmoidal" scalar nonlinearity to a linear combination of the previous states of all units. We prove that one may simulate all Turing Machines by rational nets. In particular, one can do this in linear time, and there is a net made up of about 1,000 processors which computes a universal partial-recursive function. Products	•
36 Learning Ensembles from Bites: A Scalable and Accurate Approach Nitesh V. Chawla, Lawrence O. Hall, Kevin W. Bowyer, W. Philip Kegelmeyer	
August 2004 The J urnal f Machine Learning Research, Volume 5	
Full text available: pdf(3.34 MB) Additional Information: full citation, abstract, index terms	
Bagging and boosting are two popular ensemble methods that typically achieve better accuracy than a single classifier. These techniques have limitations on massive data sets,	

because the size of the data set can be a bottleneck. Voting many classifiers built on small subsets of data ("pasting small votes") is a promising approach for learning from massive data sets, one that can utilize the power of boosting and bagging. We propose a framework for building hundreds or thousands of such classifie ... 37 The white dwarf: a high-performance application-specific processor

A. Wolfe, M. Breternitz, C. Stephens, A. L. Ting, D. B. Kirk, R. P. Bianchini, J. P. Shen May 1988 ACM SIGARCH Computer Architecture News, Proceedings of the 15th Annual International Symposium on Computer architecture, Volume 16 Issue 2 Additional Information: full citation, abstract, references, citings, index Full text available: pdf(1.40 MB) terms This paper presents the design and implementation of a high-performance special-purpose

processor, called The White Dwarf, for accelerating finite element analysis algorithms. The White Dwarf CPU contains two Am29325 32-bit floating-point processors and one Am29332 32-bit ALU, and employs a wide-instruction word architecture in which the application algorithm is directly implemented in microcode. The entire system is VME-bus compatible and interfaces with a SUN 31160 host. The syste ...

38 Computing with structured connectionist networks Jerome A. Feldman, Mark A. Fanty, Nigel H. Goddard, Kenton J. Lynne February 1988 Communications of the ACM, Volume 31 Issue 2

Additional Information: full citation, abstract, references, citings, index Full text available: pdf(1.93 MB) terms, review

The design and applications of massively parallel computational models could lead to dramatic advances in the ability to automate complex tasks such as those found in artificial intelligence.

39 Automatic subject indexing using an associative neural network Yi-Ming Chung, William M. Pottenger, Bruce R. Schatz May 1998 Proceedings of the third ACM conference on Digital libraries

Full text available: 📆 pdf(1.26 MB) Additional Information: full citation, references, citings, index terms

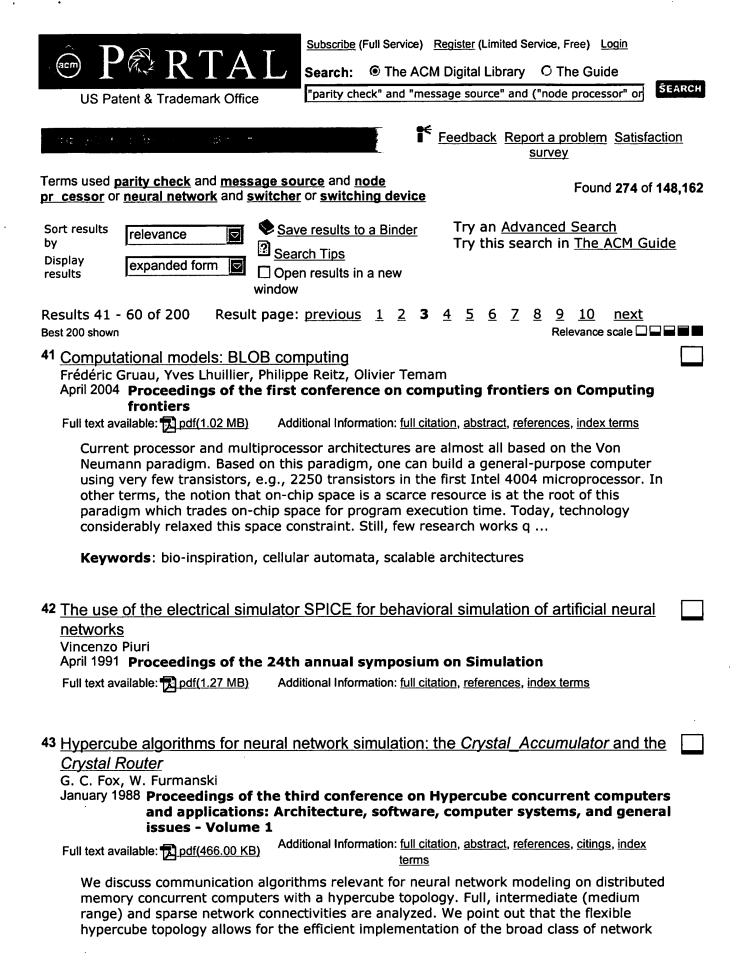
40 Analysis of a biologically motivated neural network for character recognition M. D. Garris, R. A. Wilkinson, C. L. Wilson May 1991 Proceedings of the conference on Analysis of neural network applications

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algorithms with variety of connectivity patterns. We find algorithms index, crystal_router, fold an	•
44 Artificial neural networks as cognitive tools for professional writing Patricia A. Carlson September 1990 ACM SIGDOC Asterisk J urnal f C mputer D cumentati n, Proceedings of the 8th annual international conference on Systems documentation, Volume 14 Issue 4	
Full text available: pdf(1.35 MB) Additional Information: full citation, abstract, references, index terms	
Computers are cognitive tools — they extend the capabilities of the human mind. Paper and pencil are also cognitive tools — they enhance human memory by acting as a permanent record, and they mediate the formation of thought by serving as a scratchpad or rehearsal device. However, there is a qualitative difference between these cognitive tools: the computer as a writing environment can become an active participant in the process while paper and pencil mu	1
45 Exploiting global input/output access pattern classification	
Tara M. Madhyastha, Daniel A. Reed November 1997 Proceedings of the 1997 ACM/IEEE conference on Supercomputing (CDROM)	
Full text available: pdf(232.01 KB) Additional Information: full citation, abstract, references, citings	
Parallel input/output systems attempt to alleviate the performance bottleneck that affects many input/output intensive applications. In such systems, an understanding of the application access pattern, especially how requests from multiple processors for different file regions are logically related, is important for optimizing file system performance. We propose a method for automatically classifying these global access patterns and using these global classifications to select and tune file syst	e
46 A message passing coprocessor for distributed memory multicomputers Jiun-Ming Hsu, Prithviraj Banerjee	
November 1990 Proceedings of the 1990 ACM/IEEE conference on Supercomputing Full text available: pdf(1.25 MB) Additional Information: full citation, abstract, references, citings	
This paper presents the architecture, methodology and performance evaluation of a message passing coprocessor (MPC) which can accelerate message communication in a distributed memory multicomputer. The MPC is a microprogrammable processor which offloads the CPU of the burden of communication and speeds up the software processing by directly executing message passing instructions in microcode. It supports process scheduling, message buffer management, and fast buffer copying. The most uni	
47 An approach to fault tolerance and error recovery in a parallel graph reduction	
machine: MaRS—a case study Alessandro Contessa June 1988 ACM SIGARCH Computer Architecture News, Volume 16 Issue 3	
Full text available: pdf(958.58 KB) Additional Information: full citation, abstract, index terms	
This article deals with the issue of fault tolerance and error recovery in a parallel graph reduction computer such as the "MaRS" machine presently under development at CERT. This is a multiprocessor system with decentralized control and asynchronous, delayed communications between cooperating, tightly coupled processes. A solution for the problen of MaRS error recovery is derived, based on the machine's execution model (successive reductions performed on the program graph, i.e. evaluations on t	1
A near-optimal broadcasting algorithm in all-port wormhole-routed hypercubes	

Results (page 3): "parity check" and "message source" and ("node processor" or "neural network") and (s... Page 2 of 5

Nigel Snoad, Terry Bossomaier

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December 1995 Pr ceedings f the 1995 ACM/IEEE c nference n Superc mputing

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53 Object oriented visual interactive simulation Ranko Vujosevic December 1990 Pr ceedings f the 22nd c nference n Winter simulati n	
Full text available: pdf(1.10 MB) Additional Information: full citation, references, citings, index terms	
54 <u>Architecture-independent locality-improving transformations of computational graph embedded in k-dimensions</u> Chao-Wei Ou, Manoj Gunwani, Sanjay Ranka July 1995 Proceedings of the 9th international conference on Supercomputing	<u>s</u>
Full text available: pdf(985.83 KB) Additional Information: full citation, references, citings, index terms	
55 High performance data mining (tutorial PM-3) Vipin Kumar, Mohammed Zaki August 2000 Tutorial notes of the sixth ACM SIGKDD international conference on Knowledge discovery and data mining Full text available: pdf(8.06 MB) Additional Information: full citation, references, index terms	·
56 Scheduling regular and irregular communication patterns on the CM-5 R. Ponnusamy, R. Thakur, A. Choudhary, G. Fox December 1992 Proceedings of the 1992 ACM/IEEE conference on Supercomputing Full text available: pdf(766.37 KB) Additional Information: full citation, references, citings, index terms	
57 Geometry based mapping strategies for PDE computations N. P. Chrisochoides, E. N. Houstis, C. E. Houstis June 1991 Proceedings of the 5th international conference on Supercomputing Full text available: pdf(987.17 KB) Additional Information: full citation, references, citings, index terms	
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Results (page 3): "parity check" and "message source" and ("node processor" or "neural network") and (s... Page 4 of 5

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Brian G. Kushner, John A. Neff

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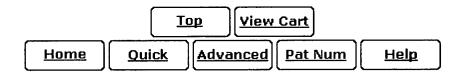


Refine Search "par

"parity check" and "message source" and ("node proces

PAT. NO. Title

- 1 4,980,857 M Operations controller for a fault tolerant multiple node processing system
- 2 4,972,415 M Voter subsystem for a fault tolerant multiple node processing system
- 3 4,933,940 In Operations controller for a fault tolerant multiple node processing system
- 4 4,914,657 In Operations controller for a fault tolerant multiple node processing system
- 5 4,561,092 Method and apparatus for data communications over local area and small area networks
- 6 4,295,218 In Error-correcting coding system





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[PPT] An Introduction to Graphical Models Kevin P Murphy Graphical ...

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Probabilities: -- The message source is given a prior distribution. where yi is the

observed message. the parity check nodes are equal to 1 iff an even.

www.cs.dartmouth.edu/~brd/Teaching/ GradAl/Students04b/graphical-models2-raz04.ppt - Similar pages

[PDF] Introduction

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... thus have two different codes of length 27 - the parity check code which Coding Theorem

which states that, beginning with an ergodic message source (such as ...

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... optimization problem for wireless com- munication applications with message source

of known be combined with the ME- codes using the parity check equation C m ...

shamir.eas.asu.edu/~mcn/ publication/yash-sourcecoding.pdf - Similar pages

[DOC] Basic Coding Theory: Error-Correcting Codes

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Using the cell phone example, the **message source** is father □s phone. An example of

a code is the Parity Check Code (8, 7). The notation (8, 7) symbolizes two ...

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In the sequel we will assume that a certain message source is already encoded through

a sequence of vectors m i 2 F k, i = 1;:::; If every vector in F k is ...

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... of data sources and optimizing it for a particular message source is not probability

calculation, let us con-sider first a simple parity-check block code.

www.comsoc.org/sac/private/ 1999/may/pdf/17sac05-turin.pdf - Similar pages

[PDF] Research NL Cover03.pmd

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... parity-check (LDPC) codes, have also emerged. Undoubtedly opportunities for research

and exploration abound in all these new territories. Message Source ...

www.science.nus.edu.sq/publications/ archv/rshlttr/deprecated/resnl-mar03.pdf - Similar pages

[PDF] Coding Theory and Applications to Communication Technologies

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All these are instances of a general communication system as in Fig. 1. message

s urc source encoder channel encoder channel channel decoder ...

pckoenig9.ma.tum.de/lehre/ic-apr2002/ic.pdf - Similar pages

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... set consisting of 7-bit coded characters (8 bits including parity check), that is The file is created from the **message s** urce file during the build process. publib.boulder.ibm.com/infocenter/iadthelp/ topic/com.ibm.etools.iseries.varpg.doc/sc092449481.htm - 46k -Cached - Similar pages

[PDF] arXiv:math.OC/9905046 v1 7 May 1999

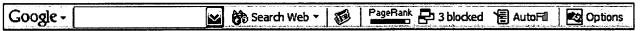
File Format: PDF/Adobe Acrobat - View as HTML In the sequel we will assume that a certain message source is already encoded through a sequence of vectors $m i \in F k$, i = 1, ..., y.

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[PDF] Codes Over Different Alphabets and Signal Sets

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Message s urce in the form of a matrix, called a generator matrix while a matrix

that repres- ents a basis for the dual code is called a parity-check matrix.

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Thus, we remove redundancy from the messages produced by the message source and

then add the right sort of redundancy to produce signal with immunity against ...

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[PS] STATISTICAL MECHANICS APPROACH TO

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of linear codes knowing the generating matrix G or the parity check matrix H) and

the ... To every possi- ble information message (source word) ~o/ we can assign a ...

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[PS] Duality between Multidimensional Convolutional

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In the sequel we will assume that a certain message source is already In the following

we want to briefly discuss parity check matrices for multidimensional ...

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[PDF] The Performance of Block Codes, Volume 49, Number 1

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... code in natural units is defined as R = (InM)/N. A message source selects one Low

Density Parity Check Codes In 1962, Gallager [5] introduced "low density par ...

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Eavesdropper Secure channel Message Source Public channel Compression Encryption

Fig. Eavesdropper Secure channel Message Source Public channel Fig.

www.eecs.berkeley.edu/~dschonbe/pubs/sp-compencryp.pdf - Similar pages

[PDF] SE 923 Scan Engine Integration Guide

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Page 1. SE 923 Scan Engine Integration Guide Page 2. 2 70-37052-01 Rev. A - February

1999 Symbol Technologies, Inc. One Symbol Plaza, Holtsville NY 11742-1300 ...

www.gotive.com/support/Manuals/3_ModulesPDF/BCR/9xx.pdf - Similar pages

грог. The problem of enciphering a message so that an enemy cryptanalyst ...

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For a given messag s urce and combiner, the design of a cipher is the Goppa codes

become cyclic and reversible after extension by an overall parity check.

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[PDF] Quantum Cryptography

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Page 1. LA-UR-95-806 Quantum Cryptography Richard J. Hughes DM Alde, P. Dyer,

GG Luther, GL Morgan and M. Schauer University of California ...

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[PDF] Communicator e3000 MPE/iX Release 7.0 (Software Release C.70.00)

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... Enhanced Message Source Template for HP 3000 Agents in ITO -- describes a new

set of source templates installed on the Management Server.

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(PDF) <u>nz i <--lb - 1 + 1 < 2" () - .</u>

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... a sequential decoder, and (for data error measurement) a replica of the message

s urce. data bits and inserts an average of (I/r - 1) parity check digits into ...

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... addresses. At each message source, the sequence of destination addresses

of the outgoing messages is compressed on a block basis.

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[PDF] Figure 1. Sherlock Holmes' "Dancing Men" which spell out the ...

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Page 2. RJ Hughes, LANL, 1994 3 key source Eve: enemy cryptanalyst message source

encryption decryption destination open channel secure channel key distribution ...

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Encrypter Message source Key source Secure channel 32 Description of DES • initial

key K : 64bit(56: key; 8: parity - 8,16, ... 64 are parity-check bits) 64 ...

csrl.gist.ac.kr/~sunihill/data/bit-cryptography.pdf - Similar pages

Patent 4354229: Loop initialization mechanism for a peer-to-peer ...

Station: A m ssage source and a sync point in the data transmission system. information

is provided in bits 0 and 5. Bits 6 and 7 are parity check bits for the ...

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2 ` 1 \Gamma C channel R ': (8) Low Density Parity Check Codes - A Statistical

Physics Prospective 10 a prior distribution for the message source P (s).

www.cs.huji.ac.il/.../p2p/resources/ low-density-parity-check-codes-a-statistical-physics-perspective.ps - Similar pages

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Page 1. Aspects of Cryptography and Internet Security Sanna Jäälinoja The University

of Oulu The Department of Mathematical Sciences M.Sc. thesis Page 2.2 ...

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[PDF] Z/OS V1R6.0 MVS System Messages, Vol 1 (ABA-AOM)

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S urce: Extended remote copy (XRC). System Action: The command is canceled. S urc :

Extended remote copy (XRC). System Action: The command is canceled.

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Integrity also contains of non-repudiation of a m ssage s urc , which will described

later. data is striped across several drives and the parity check bit is ...

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United States Patent Application: 0040054960

... of a communications system configured to utilize Low Density **Parity Check** (LDPC) codes ... system 100, the transmitter 101 has a **message source** that produces a ... appft1.uspto.gov/netacgi/nph-Parser?Sect1=PTO2& Sect2=HITOFF&p=2&u=%2Fnetahtml%2FPTO%2Fsearch-... - 101k - Supplemental Result - <u>Cached</u> - <u>Similar pages</u>

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[PS] Carl von Ossietzky Universita"t Oldenburg

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We assume that a certain message source is represented by the vectors in F k rator

matrix and Ha parity check matrix of C. Generator matrix and parity check ...

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